

Demo EMS Logger

The World Health Organization's Immunization and Medical Devices - Performance Quality, and Safety group (WHO IMD-PQS) has published a set of specifications collectively known as the Equipment Monitoring System (EMS). These specifications define functionality for the next generation of cold chain equipment (CCE) monitoring solutions. The set contains three related specifications and their associated verification protocols

The Demonstration EMS Logger is a sample implementation of the WHO/PQS/E006/DL01 specification. That is, it collects temperature, door opening, and power system data from the CCE and stores it for at least one year. It is intended to serve as a test of the specification and its verification protocol. During the design and evaluation process, New Horizons has been looking for areas where the specification can be clarified. The device can also serve as a reference design for others implementing the DL01 specification.

Please refer to the description of the motivations and operation of the circuit, which should be part of the materials of this package. If you did not receive these materials, the whole package may be downloaded from <https://docs.2to8.cc>.

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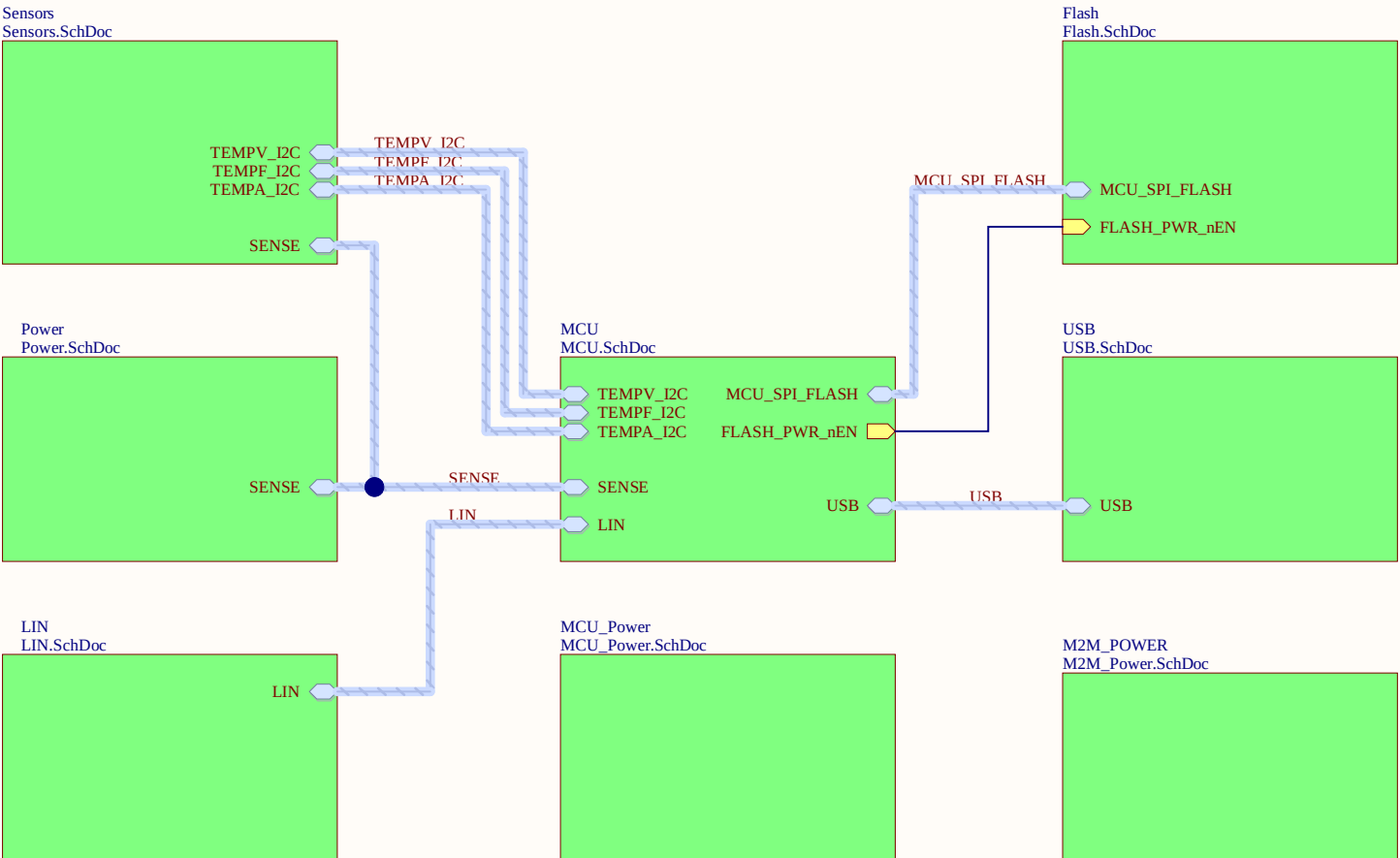
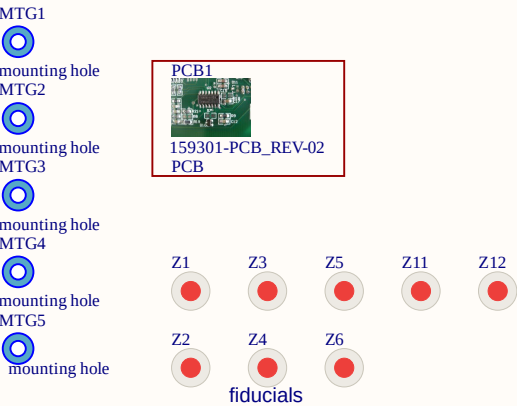
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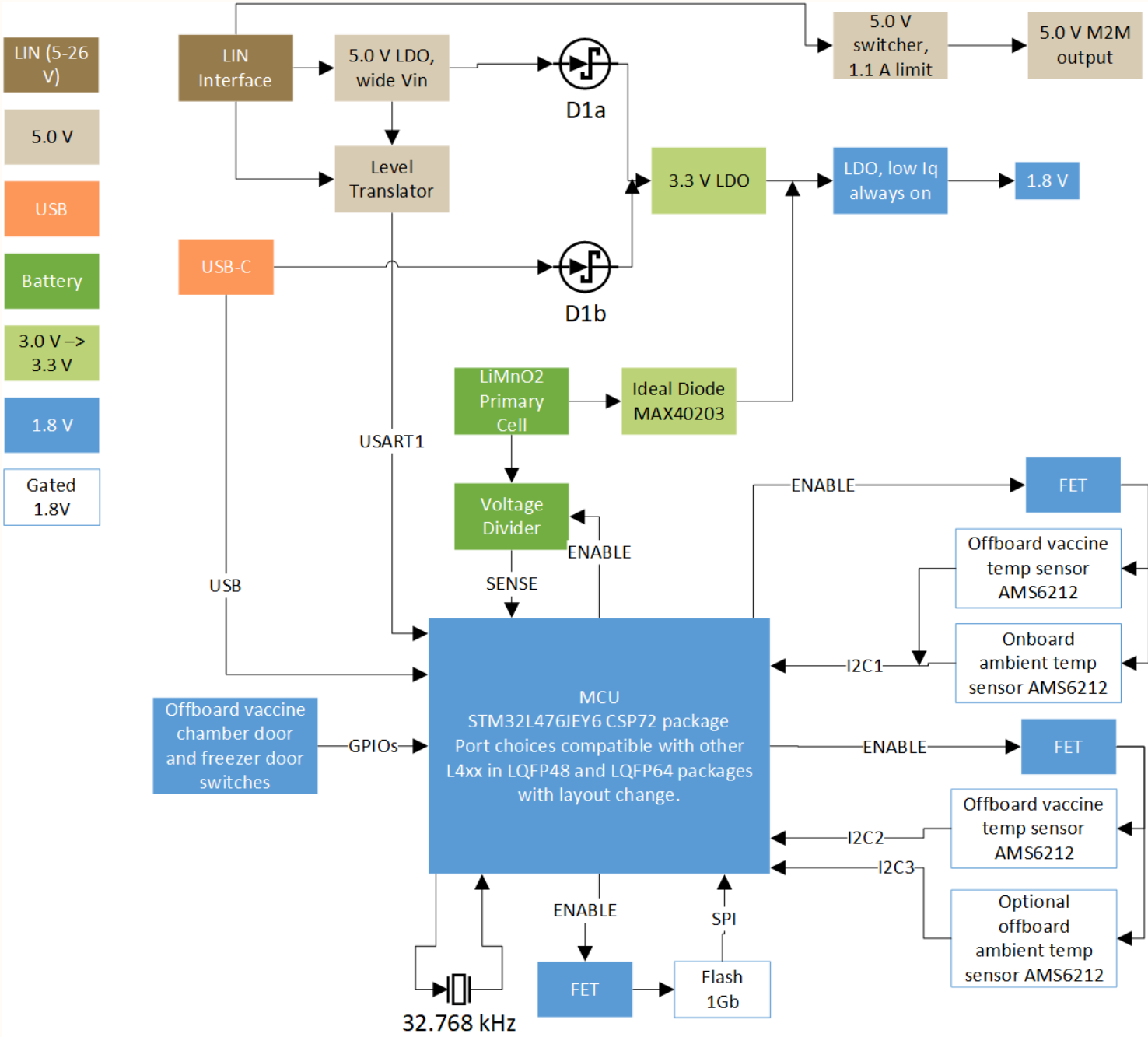
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PCB Design Rules based on Royal Circuits DFM consultation:

- * Created a room around the uC BGA which makes a class with just the uC in it. Called it "FanoutRoom" and used it in other rules for fanout control. Note that the room and associated class definition were created in the PCB editor, so every time you update from schematics, you need to uncheck the "delete room" and "delete class" line items in the ECO or we will lose the definition.
- * Created a clearance rule for objects within the fanout room for 3.25 mil spacing. In layout, we will try to space things 6 mils, but this rule allows for microvias clearances.
- * Note that I have retained an inner layer clearance rule of 10 mils from Sunstone's requirements, though we could go to 6 mils per Royal Circuits' capabilities table.
- * Created a via rule within the fanout room with 5.1 mil hole through-hole and 12 mil pad diameter, the smallest drilled hole Royal Circuits will do. Restrict this small via to fanout to keep costs down. Through-hole vias outside the room are relatively easy to fab: 14 mil hole and 32 mil copper.
- * Created a microvia rule within the fanout room with 4 mil diameter hole and 8 mil copper, the smallest Royal Circuits is comfortable with. Microvias outside the room are also 4 mils, but have 12 mil copper to increase the annular ring.
- * Changed the solder mask expansion rule from 4 mils to 2 mils, so that all footprints that depend on the rule will use that expansion. Manually set ones will not.
- * I changed the default component clearance rule from 10 mil to 4 mil (this change was not communicated to Royal Circuits).

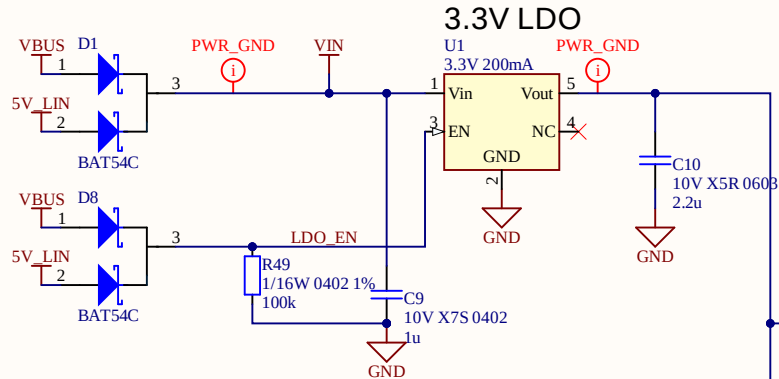


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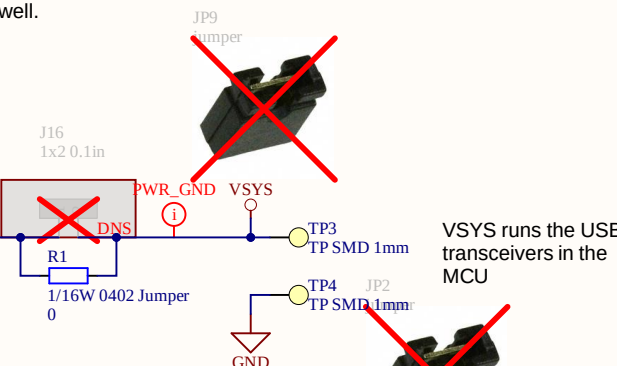
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Diodes remove reverse current path through LDO--expected typical reverse leakage should be well under 1uA at 85C. Also, isolates power input from different sources.

Separate diode pair for enable input (EN) to keep regulator in low power state when even though there will be back conduction through its pass FET.



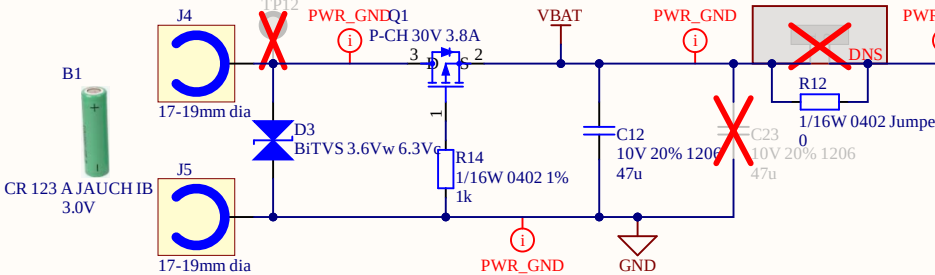
This output capacitor shares double duty bypassing the output of the Ideal Diode as well.



VSYS runs the USB transceivers in the MCU

Battery

FET based reverse polarity protection; FET has very low leakage through gate (good for battery life)



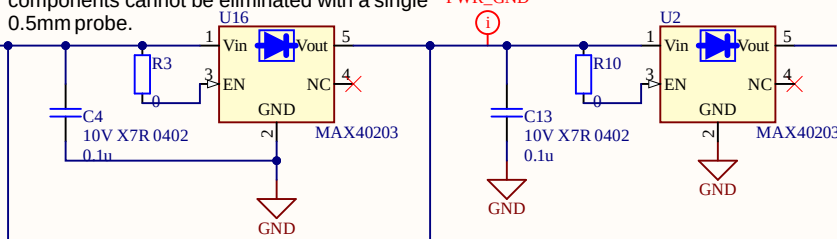
Low leakage ESD diode; Bidirectional to work with the possible reverse polarity condition.

UL Compliant Protection

UL requires redundant protection of battery for potential reverse current. We layout three options due to part shortages and solution features. The 'test' is for a short of 0.5mm in size. So, it is sufficient to make sure that both protection components cannot be eliminated with a single 0.5mm probe.

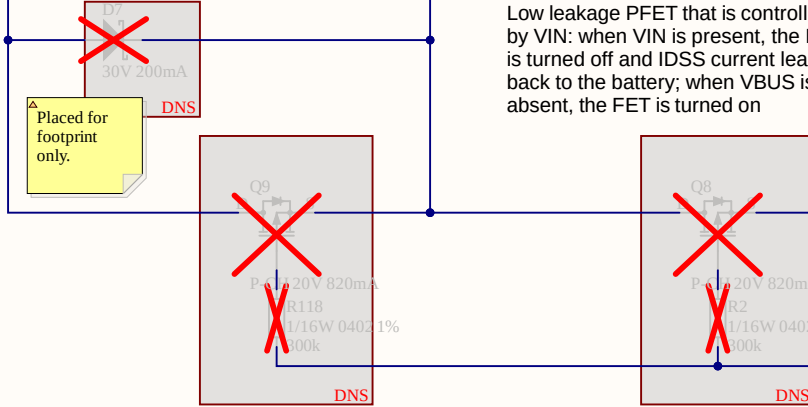
Ideal Diode

Extremely low reverse leakage current to avoid charging battery (easier to spec than equivalent FET circuit).



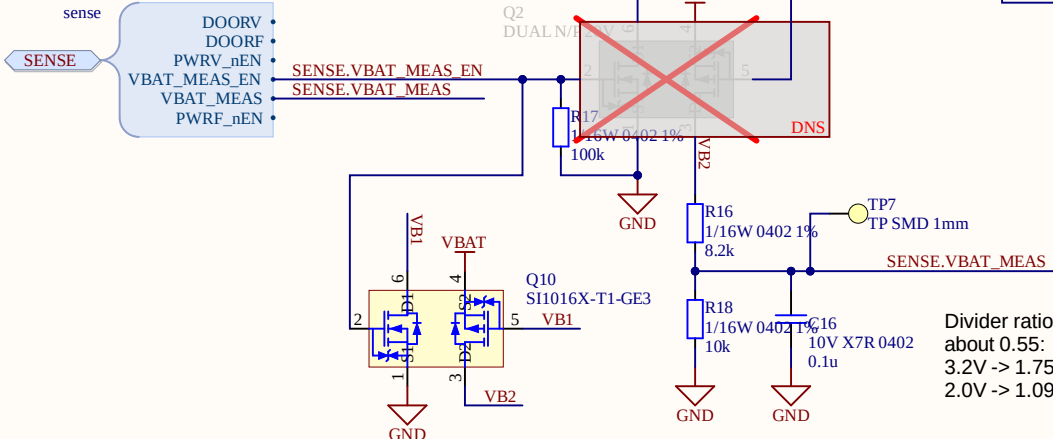
Alternate Power Path

Low leakage PFET that is controlled by VIN: when VIN is present, the FET is turned off and IDSS current leaks back to the battery; when VBUS is absent, the FET is turned on



DMG1013UW
rated for IDSS -100nA max
rated for IGSS -2uA max
Graphs show likely leakages far lower.
Even with these values, the battery life and protection should be OK.

DMG2305U
-1uA max IDSS, however table shows we should expect less than 100nA (i.e. how much current leaks back into battery)
+/-100nA max IGSS (leakage we'll see from VSYS to GND)

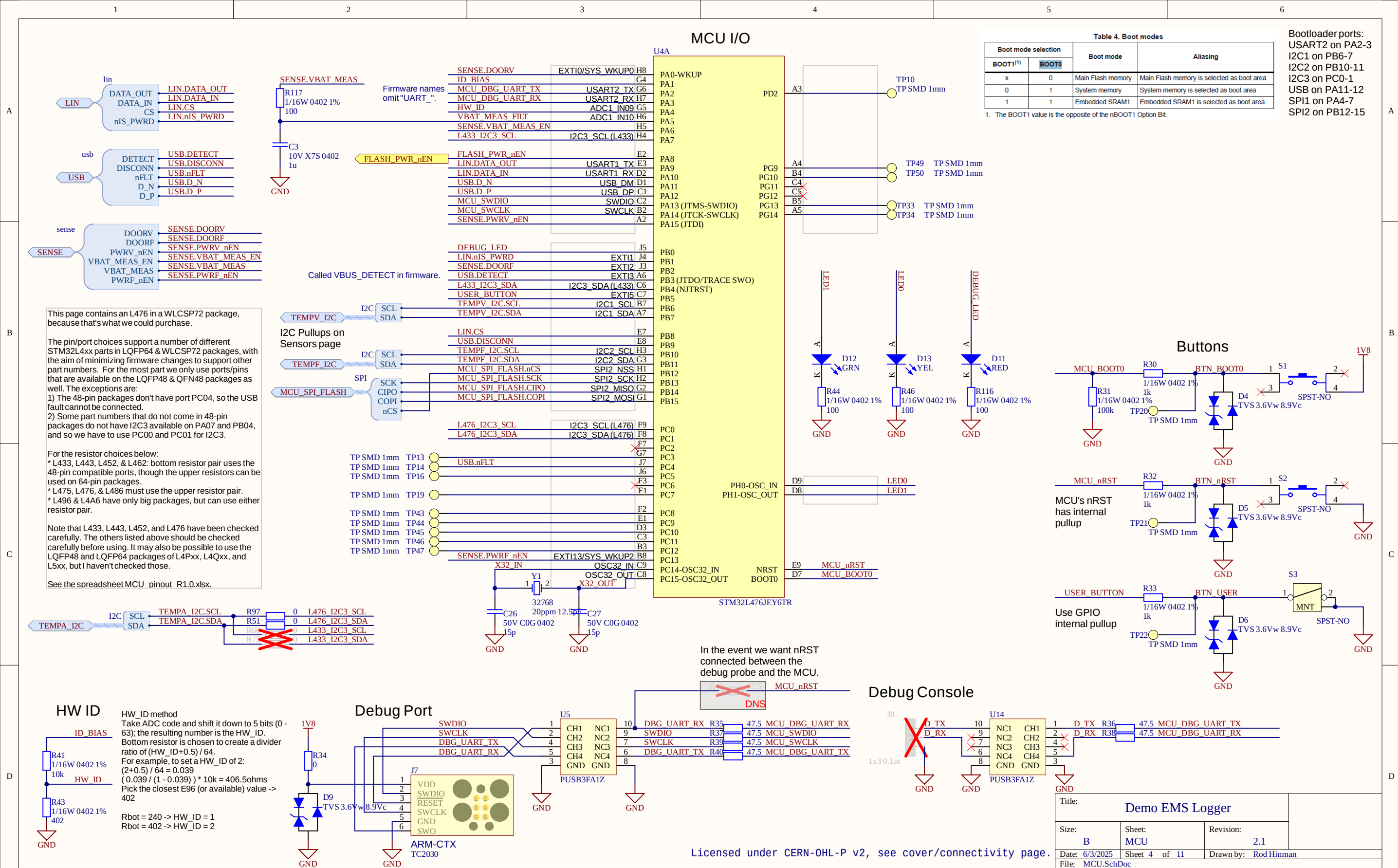


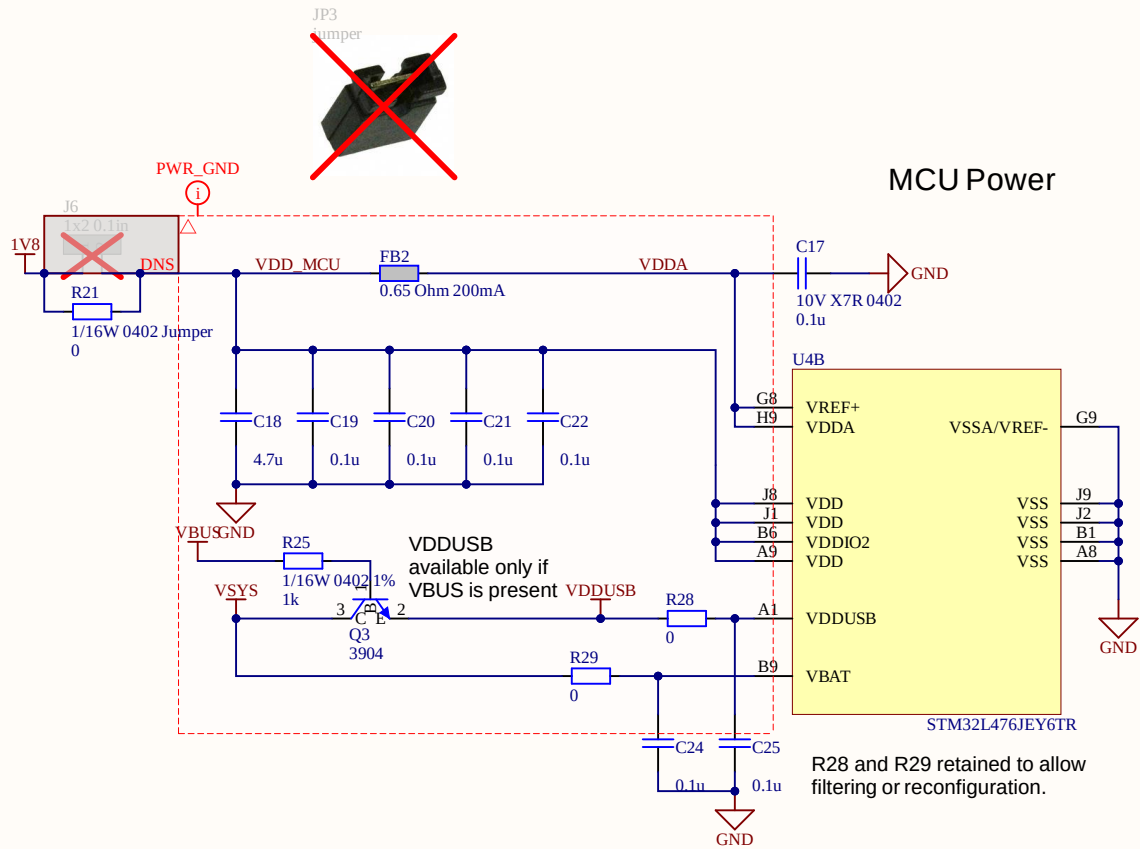
Battery Measurement with alt. packages

Divider ratio is about 0.55:
3.2V -> 1.758V
2.0V -> 1.099V

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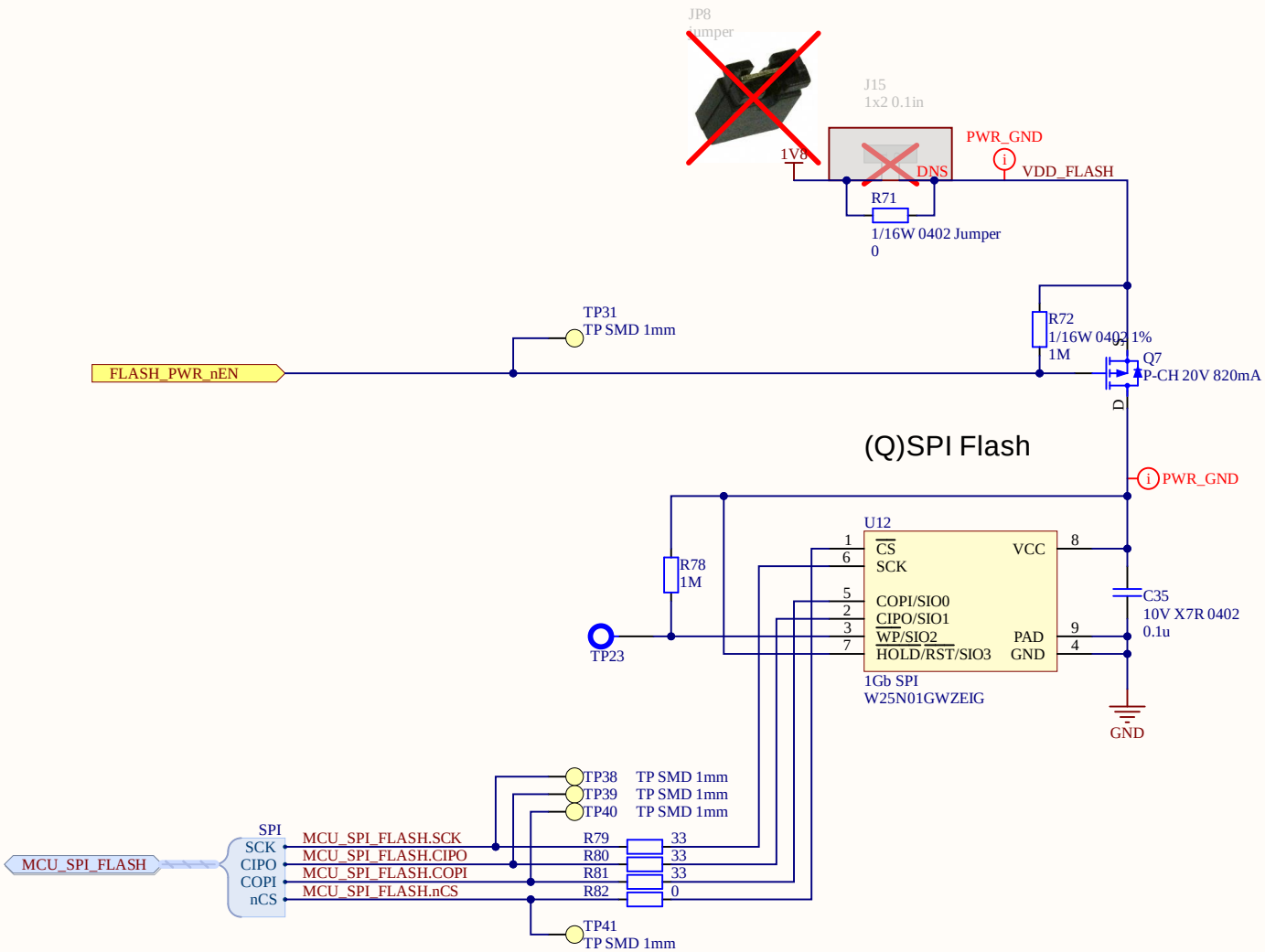
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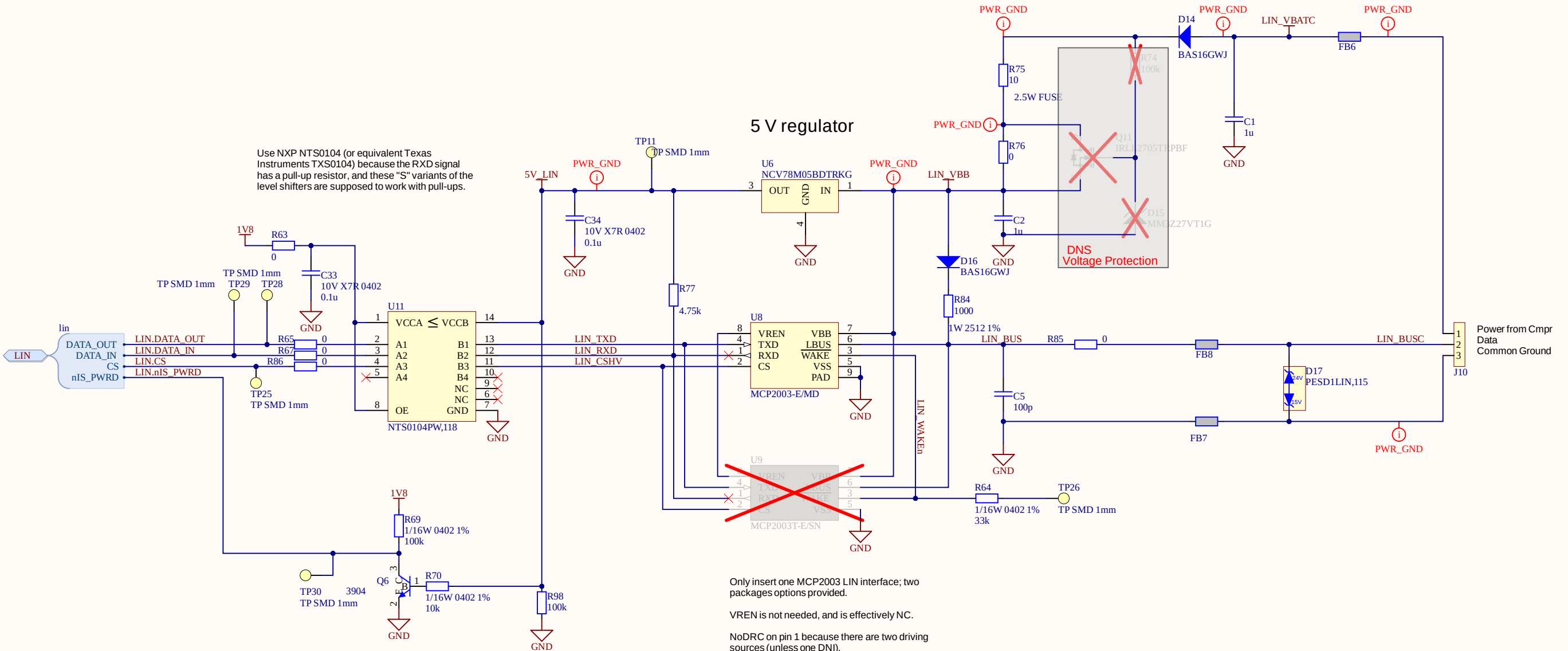
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LIN/MODBUS

LIN signal voltage range: 5.0 V to 27.0 V, and
MCP2003 supply range 6.0 V to 27.0 V.

If powering from a regulated 24 V supply, you can
the omit voltage protection components.

If powering from PV where Vpv > 27 V, use
voltage protection components and omit R76 to
work with up to 72-cell modules (58 V).



5 V regulator

Use NXP NTS0104 (or equivalent Texas
Instruments TXS0104) because the RXD signal
has a pull-up resistor, and these "S" variants of the
level shifters are supposed to work with pull-ups.

DNS
Voltage Protection

Only insert one MCP2003 LIN interface; two
packages options provided.

VREN is not needed, and is effectively NC.

NoDRC on pin 1 because there are two driving
sources (unless one DNI).

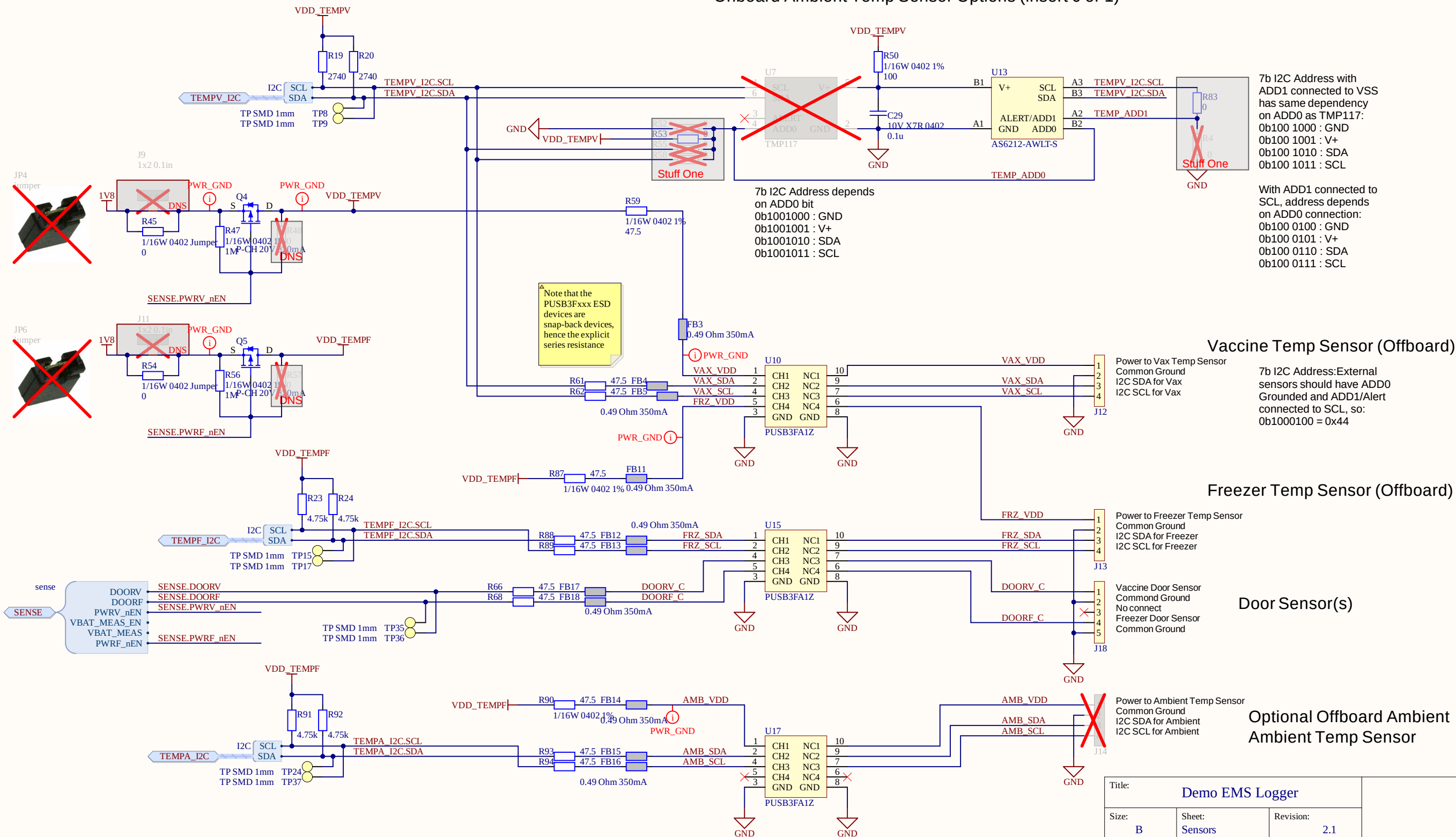
WAKEn is pulled up internally. Test point provided
in case we need to pull it down to wake.

R84 1K 1W pull-up for LIN bus master.

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Onboard Ambient Temp Sensor Options (insert 0 or 1)

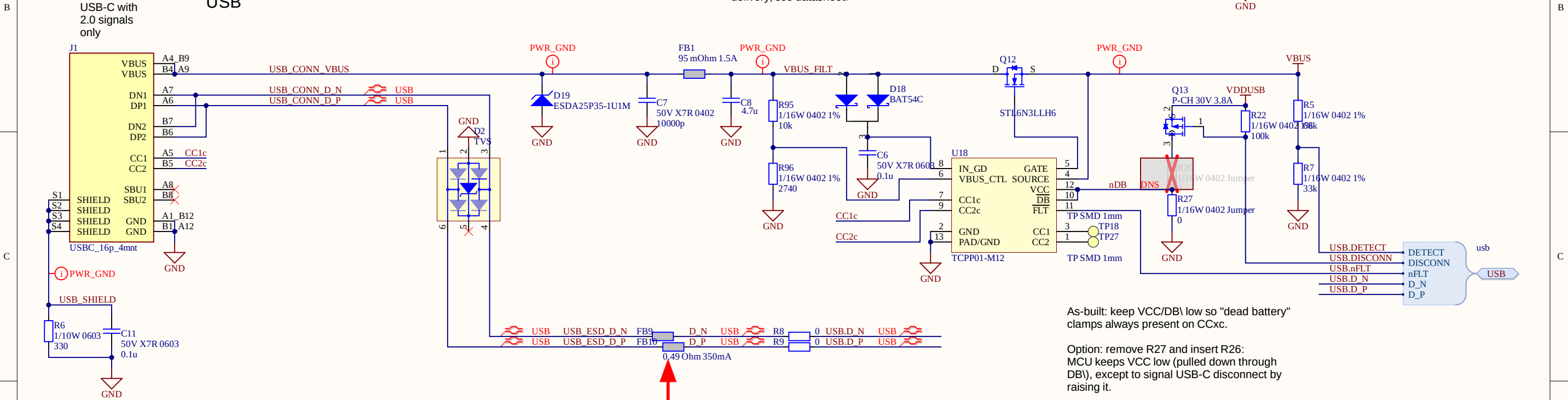
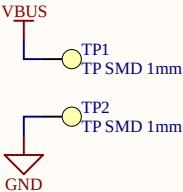


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VBUS overvoltage protection triggered when $V_{in} > (R_x/R_y + 1) * V_{bus_ctrl}$.

Data sheet shows $1.20\text{ V} \leq V_{bus_ctrl} \leq 1.34\text{ V}$ (nominal 1.25 V), so with 1% resistors included (but most of the variation is from the IC)
:
 $4.29\text{ V} \leq \text{VBUS OVP} \leq 6.33\text{ V}$ (nominal 5.8 V)

Capacitors not needed on CCxc because not using power delivery, see datasheet.



Note pin 5 of D2 is disconnected because it won't survive 20V from power delivery applied, but D19 will.

For future revisions:

FB9 and FB10 slow data signal rise times so that they are outside the USB Full Speed specification (but still work with most USB hosts). Future revisions should consider changing to a single common-mode choke or an integrated common-mode filter and ESD protection device.

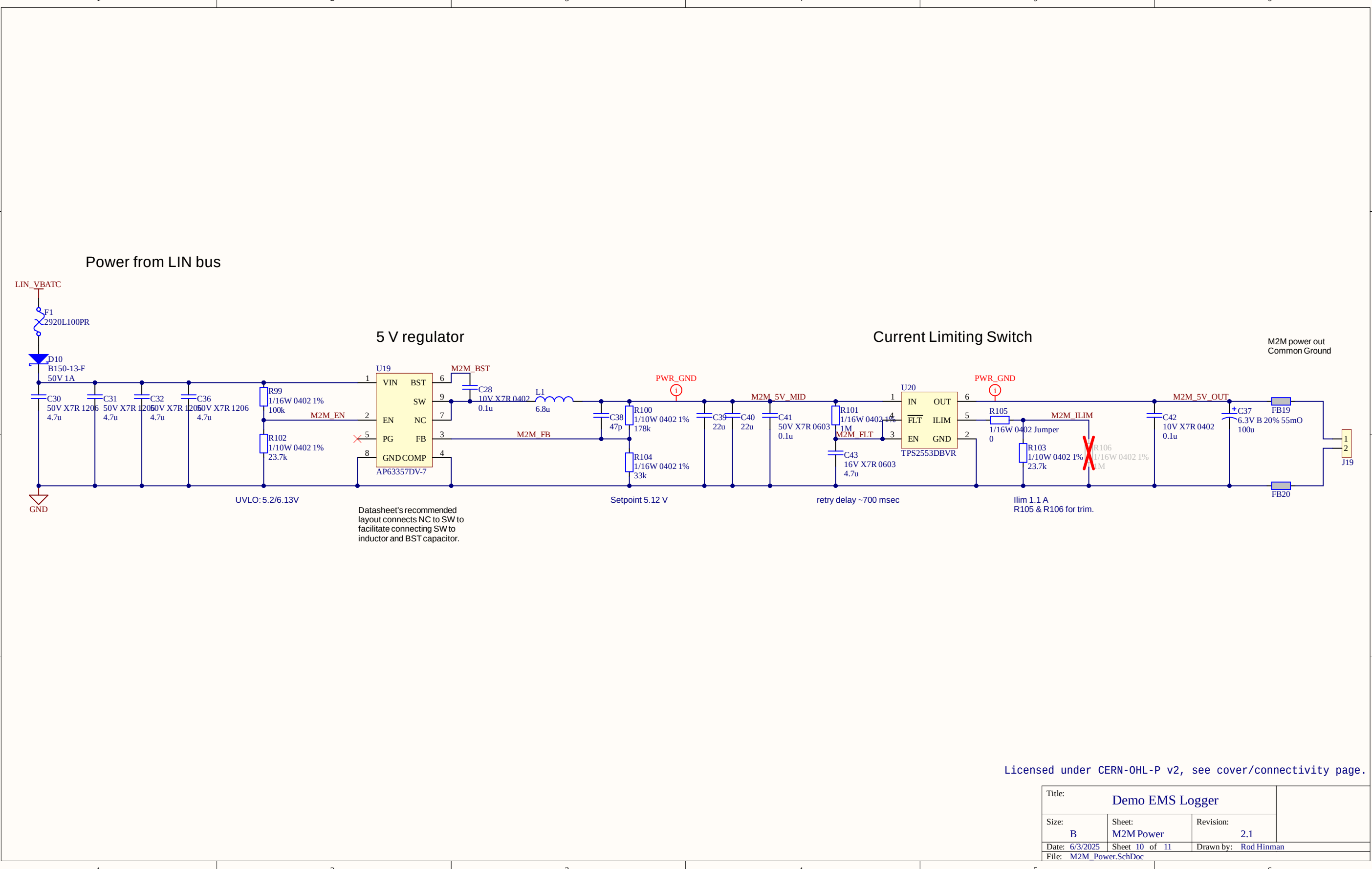
As-built: keep VCC/DB\ low so "dead battery" clamps always present on CCxc.

Option: remove R27 and insert R26: MCU keeps VCC low (pulled down through DB\), except to signal USB-C disconnect by raising it.

VDDUSB gets pulled to 3.3V when VBUS is present, so PB09 = USB.DISCONN does get pulled above 1.8V. It is a 5V tolerant pin, so should be OK.

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	CHANGE HISTORY																									
	REV	DATE	BY	DESCRIPTION OF CHANGE																						
	01	2022-08-12	Rod Hinman	Initial Release (note manufacturing files produced 2022-07-22; subsequent changes documentation only).																						
	02	2023-12	Rod Hinman	Added M2M Power output.																						
02.1	2025-05-20	Rod Hinman	License info and other documentation for open sourcing.																							
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